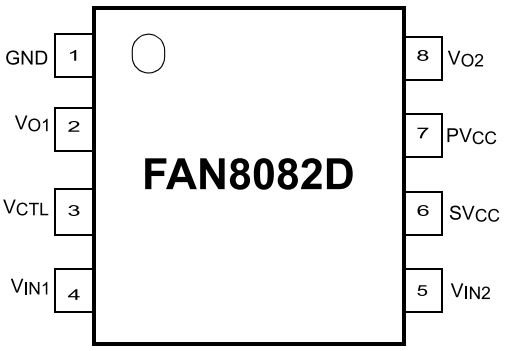
8. IC Block Diagrams

8-1 Main

8-1-1. FAN8082D

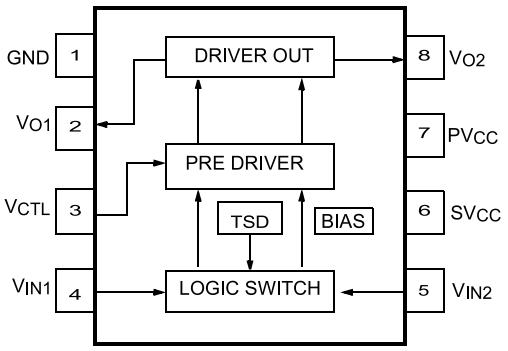
Pin Assignments



Pin Definitions

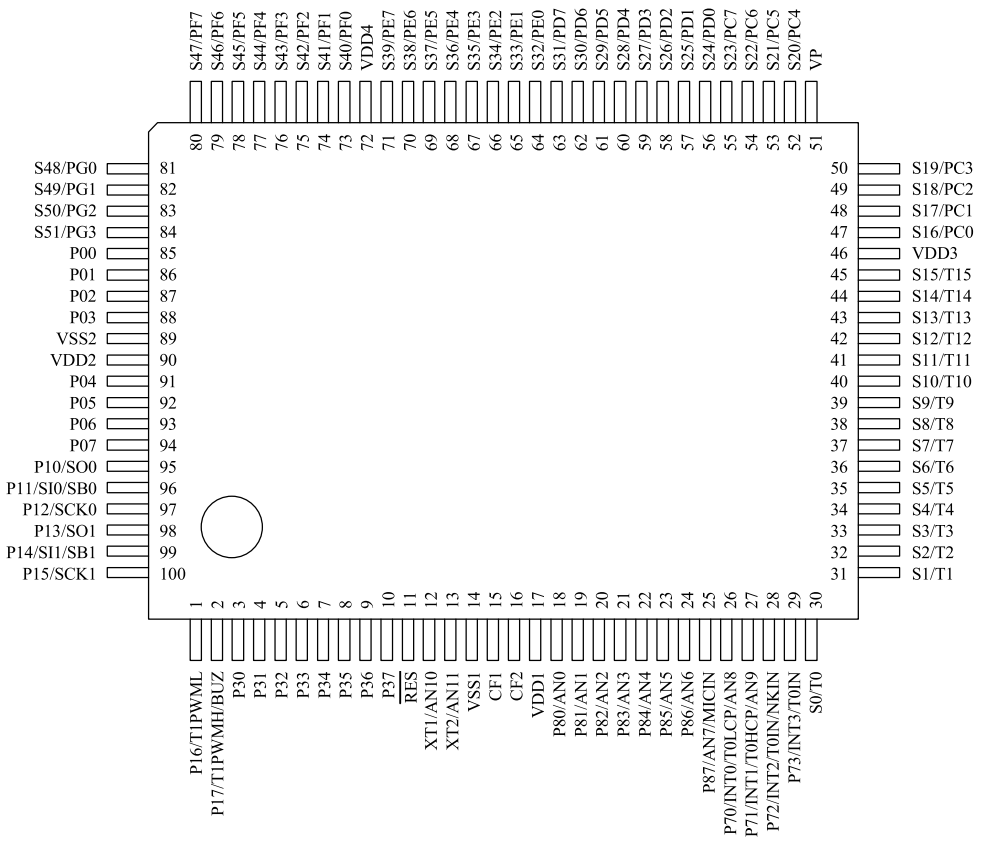
Pin Number	Pin Name	I/O	Pin Function Description
1	GND	-	Ground
2	V_{O1}	O	Output 1
3	V_{CTL}	I	Motor speed control
4	V_{IN1}	I	Input 1
5	V_{IN2}	I	Input 2
6	SV_{CC}	-	Supply voltage (Signal)
7	PV_{CC}	-	Supply voltage (Power)
8	V_{O2}	O	Output 2

Internal Block Diagram



LC87F66C8A

Pin Assignment

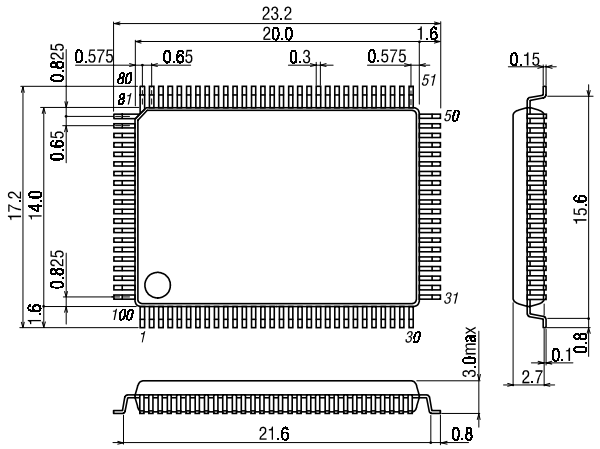


SANYO: QIP-100E

Package Dimensoin

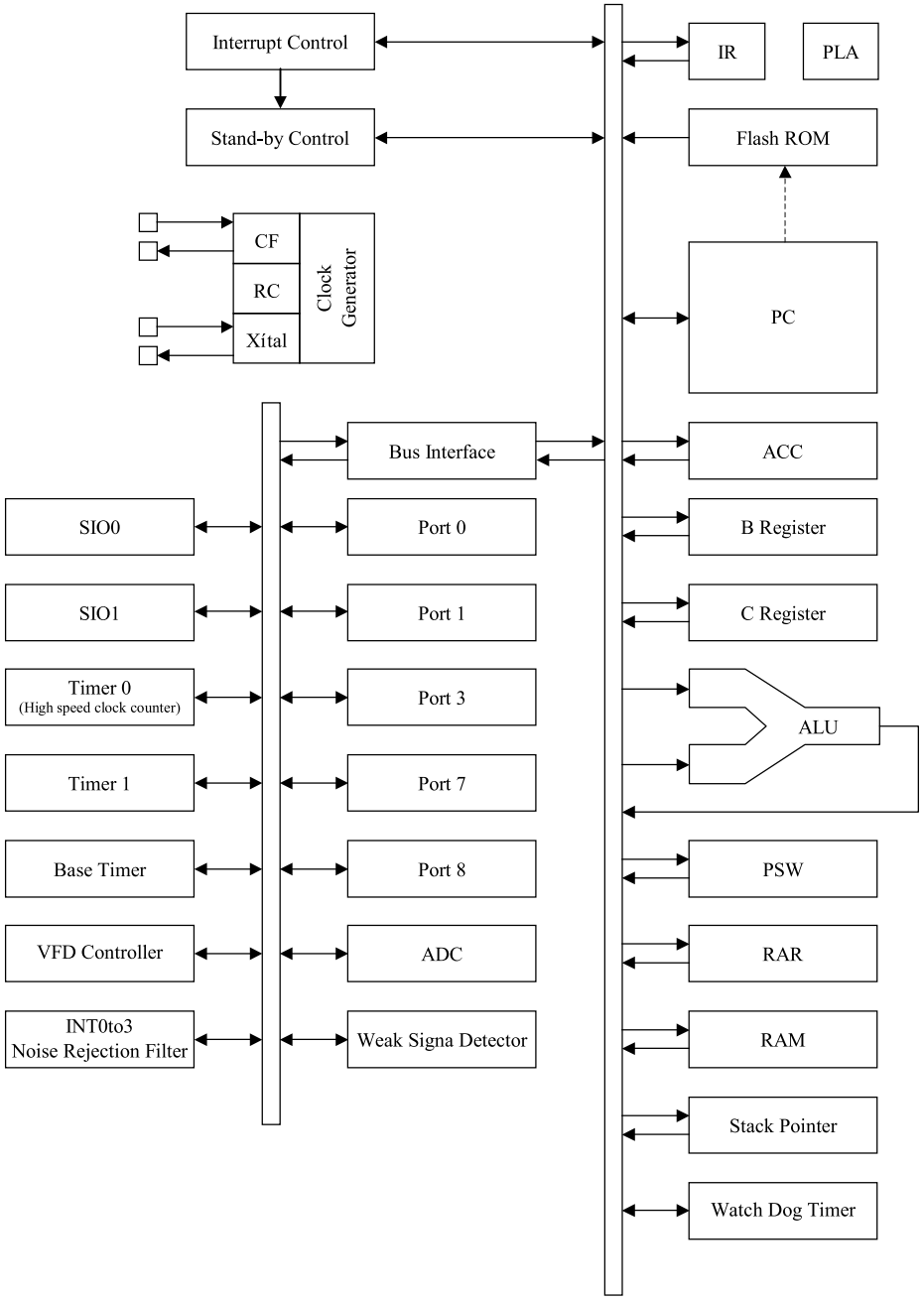
(unit : mm)

3151



SANYO: QIP-100E

System Block Diagram

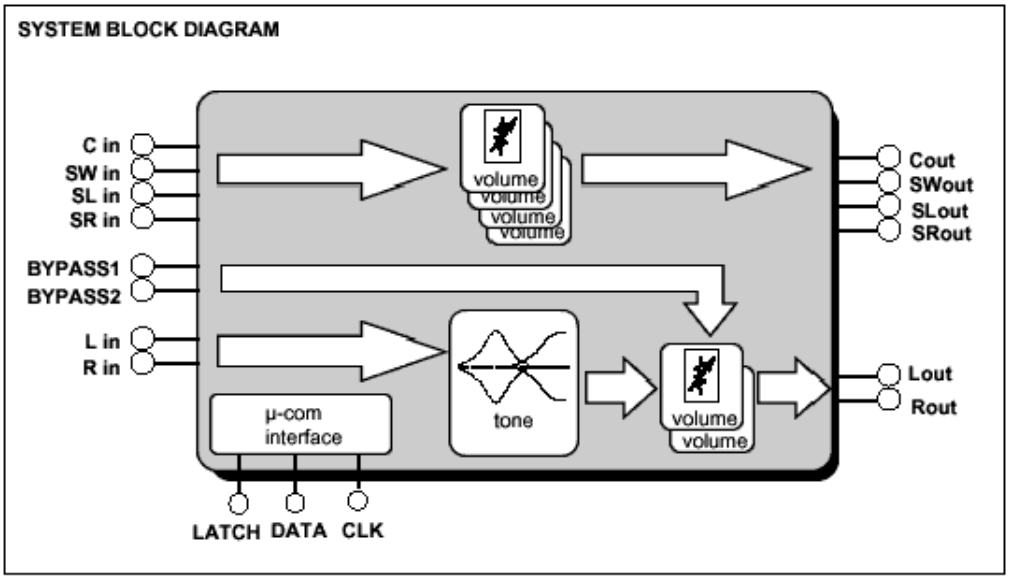


Pin Assignment

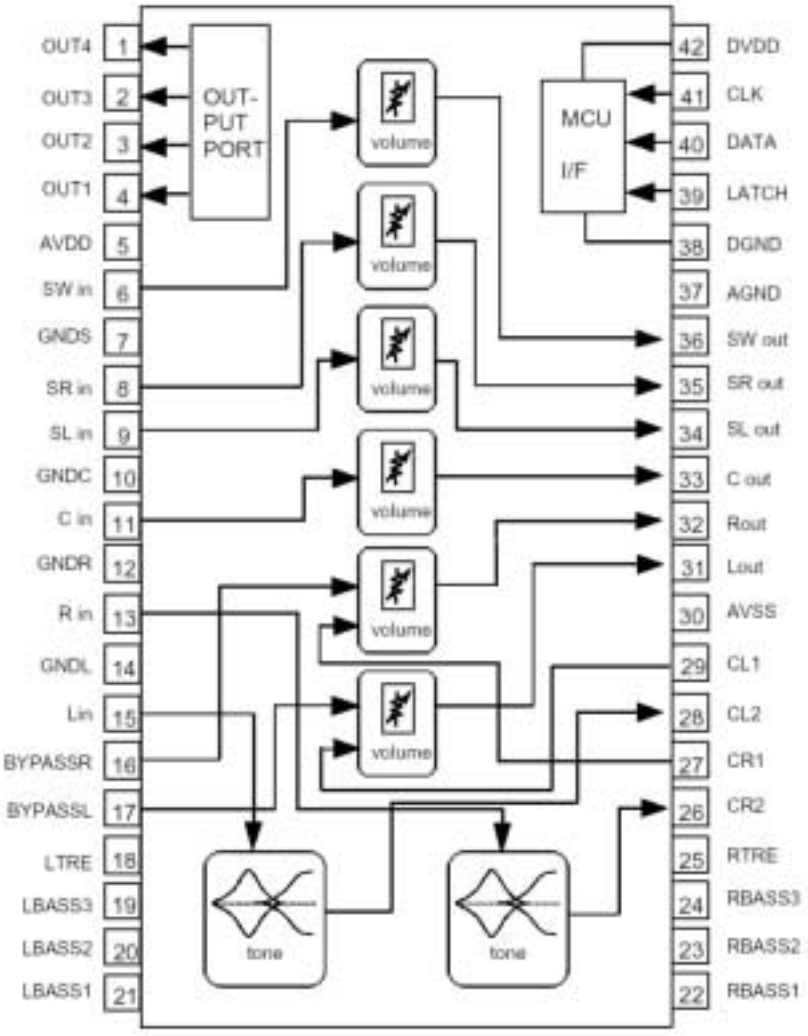
<table>
<tr><th>Pin name</th><th>I/O</th><th>Function</th><th>Option</th></tr>
<tr><td>VSS1
VSS2</td><td>-</td><td>□Power supply (-)</td><td>No</td></tr>
<tr><td>VDD1
VDD2
VDD3
VDD4</td><td>-</td><td>□Power supply (+)</td><td>No</td></tr>
<tr><td>VP</td><td>-</td><td>□Power supply (-)</td><td>No</td></tr>
<tr><td>PORT0
P00 to P07</td><td>I/O</td><td>□8bit input/output port
□data direction programmable in nibble units
□Use of pull-up resistor can be specified in nibble units
□Input for HOLD release
□Input for port 0 interrupt
□15V withstand at N-channel open drain output</td><td>Yes</td></tr>
<tr><td>PORT1
P10 to P17</td><td>I/O</td><td>□8bit input/output port
□data direction programmable for each bit
□Use of pull-up resistor can be specified for each bit
□Other pin functions
P10 SIO0 data output
P11 SIO0 data input/bus input/output
P12 SIO0 clock input/output
P13 SIO1 data output
P14 SIO1 data input/bus input/output
P15 SIO1 clock input/output
P16: Timer 1 PWML output
P17: Timer 1 PWMH output/Buzzer output</td><td>Yes</td></tr>
<tr><td>PORT3
P30 to P33</td><td>I/O</td><td>□8bit Input/output port
□Data direction can be specified for each bit
□Use of pull-up resistor can be specified for each bit
□15V withstand at N-channel open drain output</td><td>Yes</td></tr>
<tr><td>PORT7
P70 to P73</td><td>I/O</td><td>□4bit Input/output port
□Data direction can be specified for each bit
□Use of pull-up resistor can be specified for each bit
□Other functions
P70: INT0 input/HOLD release input/Timer0L capture Input/output for watchdog timer
P71: INT1 input/HOLD release input/Timer0H capture input
P72: INT2 input/HOLD release input/timer 0 event input/Timer0L capture input/High speed clock counter input
P73: INT3 input(noise rejection filter attached input)/timer 0 event input/Timer 0H capture input
AD input port: AN8(P70), AN9(P71)
The following types of interrupt detection are possible:
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising/ falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT1</td><td>Yes</td><td>Yes</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>INT2</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
<tr><td>INT3</td><td>Yes</td><td>Yes</td><td>Yes</td><td>No</td><td>No</td></tr>
</table></td><td>No</td></tr>
</table>

Pin name	I/O	Function description	Option
PORT8 P80 to P87	I/O	□8bit Input/output port □Input/output can be specified in a bit unit □Other functions: AD input port: AN0 to AN7 Weak signal detector input port: MICIN(P87)	No
S0/T0 to S8/T8	O	□Large current output for VFD display controller digit (can be used for segment)	No
S9/T9 to S15/T15	O	□Large current output for VFD display controller segment/digit	No
S16 to S23	I/O	□Output for VFD display controller segment/digit □Other functions: High voltage input port: PC0 to PC7	No
S24 to S31	I/O	□Output for VFD display controller segment □Other functions: High voltage input port: PD0 to PD7	No
S32 to S39	I/O	□Output for VFD display controller segment □Other functions High voltage input port: PE0 to PE7	No
S40 to S47	I/O	□Output for VFD display controller segment □Other functions: High voltage input/output port: PF0 to PF7	No
S48 to S51	I/O	□Output for VFD display controller segment □Other functions: High voltage input/output port: PG0 to PG3	No
$\overline{\text{RES}}$	I	Reset terminal	No
XT1	I	□Input for 32.768kHz crystal oscillation □Other functions: General purpose input port When not in use, connect to VDD1. AD input port: AN10	No
XT2	I/O	□Output for 32.768kHz crystal oscillation □Other functions: General purpose input port When not in use, set to oscillation mode and leave open circuit. AD input port: AN11	No
CF1	I	Input terminal for ceramic oscillator	No
CF2	O	Output terminal for ceramic oscillator	No

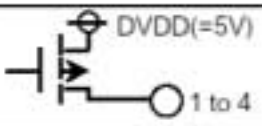
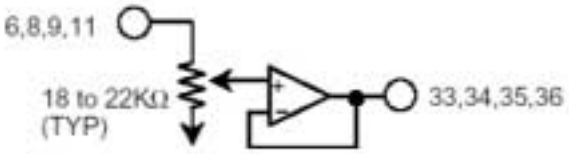
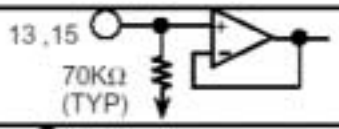
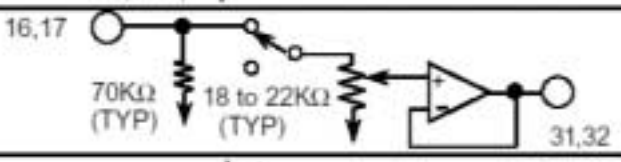
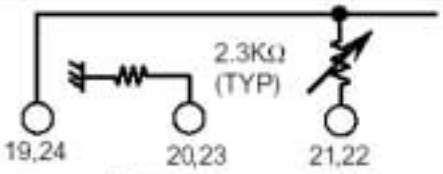
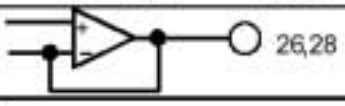
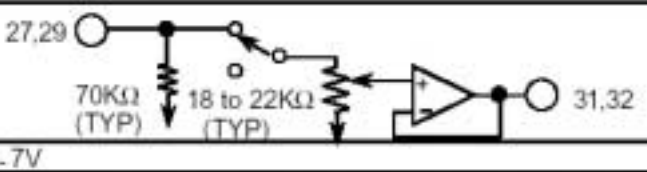
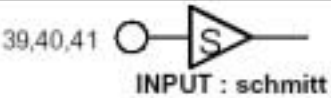
8-1-3. M62446AFP



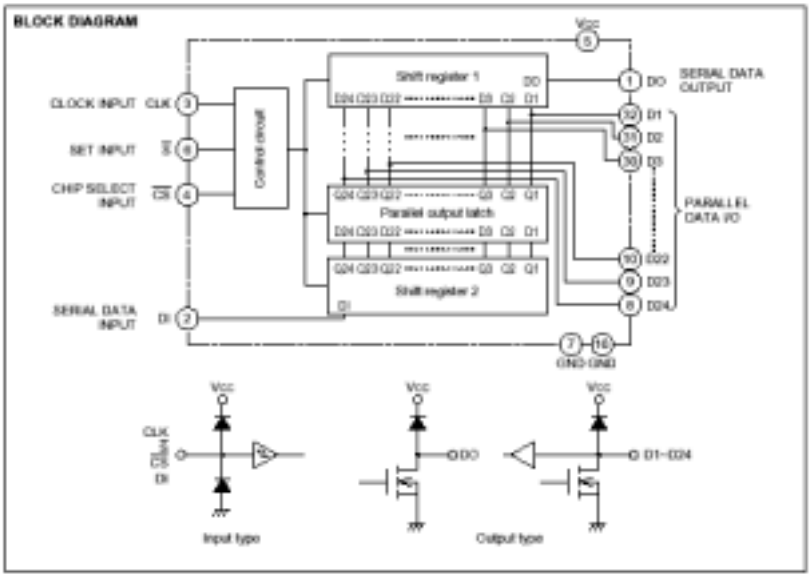
PIN CONFIGURATION AND BLOCK DIAGRAM



PIN DESCLIPTION

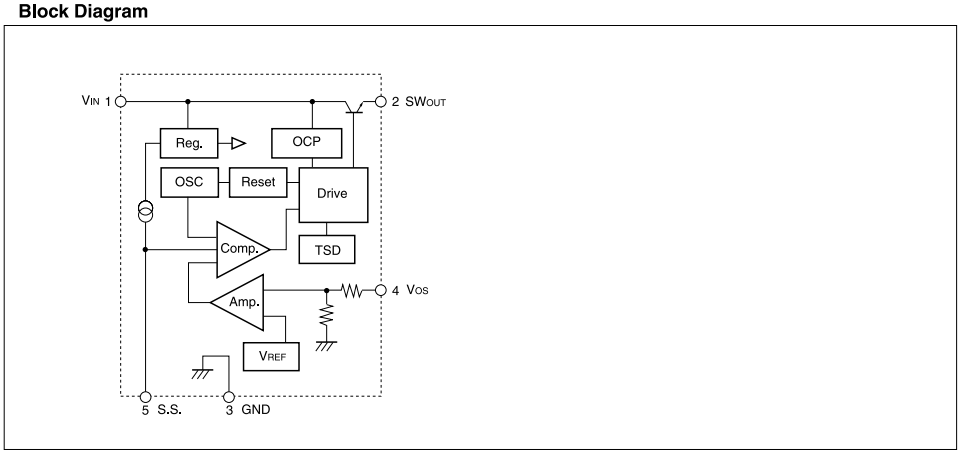
Pin No.	Symbol	Function	Circuit
1 2 3 4	OUT4 OUT3 OUT2 OUT1	Port OUTPUT	OUTPUT:PMOS Transistor open drain 
5	AVDD	Analog positive Power supply	+7V
7 10 12 14	GNDS GNDC GNDR GNDL	GND	Connect to analog GND
6 8 9 11	SW in SR in SL in C in	Volume INPUT	
36 35 34 33	SW out SR out SL out C out	Volume OUTPUT	
13 15	R in L in	Tone INPUT	
16 17 31 32	BYPASSR BYPASSL Lout Rout	L,R Volume INPUT in BYPASS mode L OUTPUT R OUTPUT	
18 25	LTRE RTRE	tone Treble cycle control	
19 24 20 23 21 26	LBASS3 RBASS3 LBASS2 RBASS2 LBASS1 RBASS1	tone Bass cycle control	
22 28	CR2 CL2	Tone OUTPUT	
27 29 31 32	CR1 CL1 Lout Rout	L,R Volume INPUT L OUTPUT R OUTPUT	
30	AVSS	Analog negative Power Supply	-7V
37	AGND	Analog GND	
38	DGND	Digital GND	
39 40 41	LATCH DATA CLK	Latch INPUT Data INPUT Clock INPUT Forward data	 **INPUT : schmitt trigger type**
42	DVDD	Digital Power supply	+5V

8-1-4. M66010FP



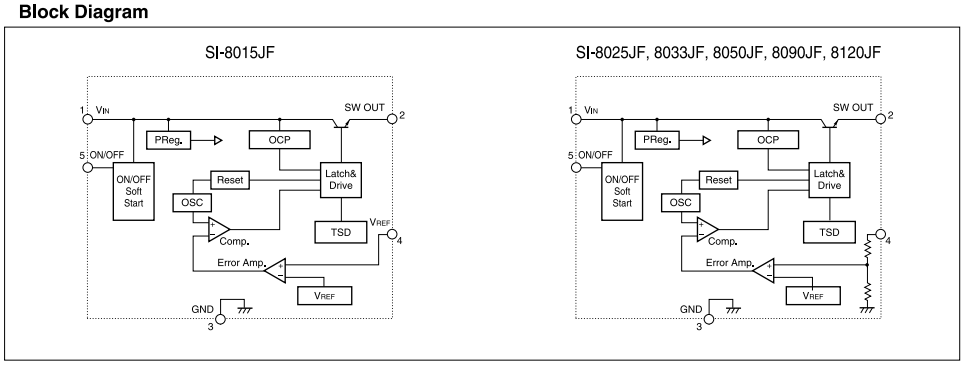
8-1-5. SI-8050SE

Block Diagram



8-1-6. SI-8090JFE

Block Diagram



Block Diagram

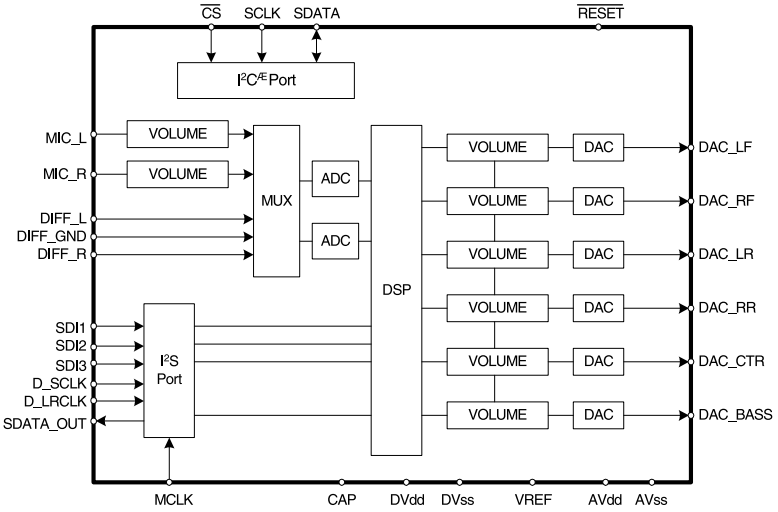
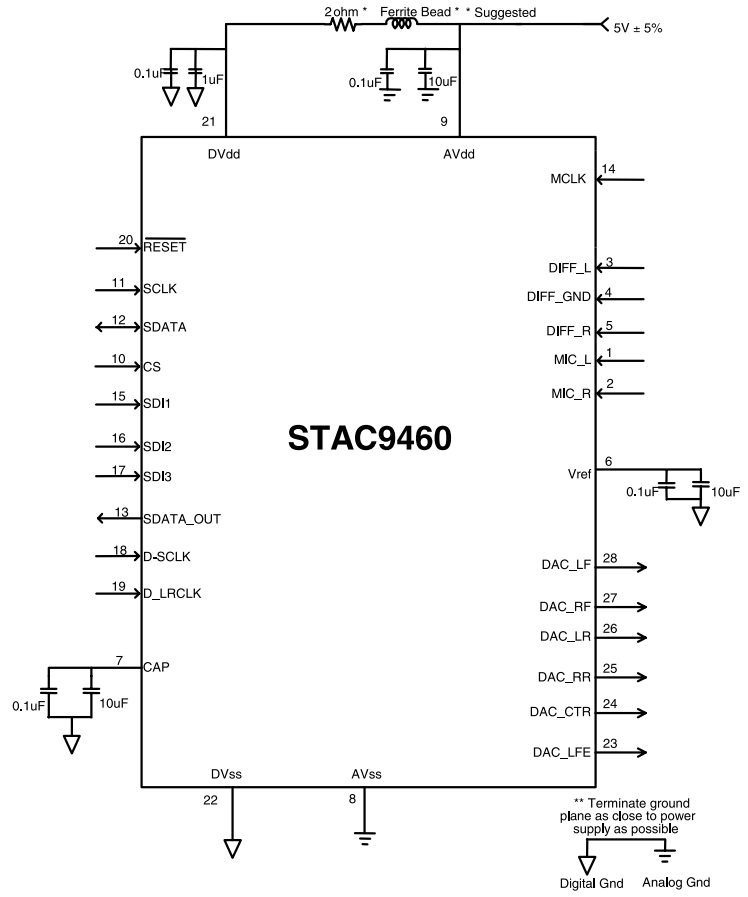
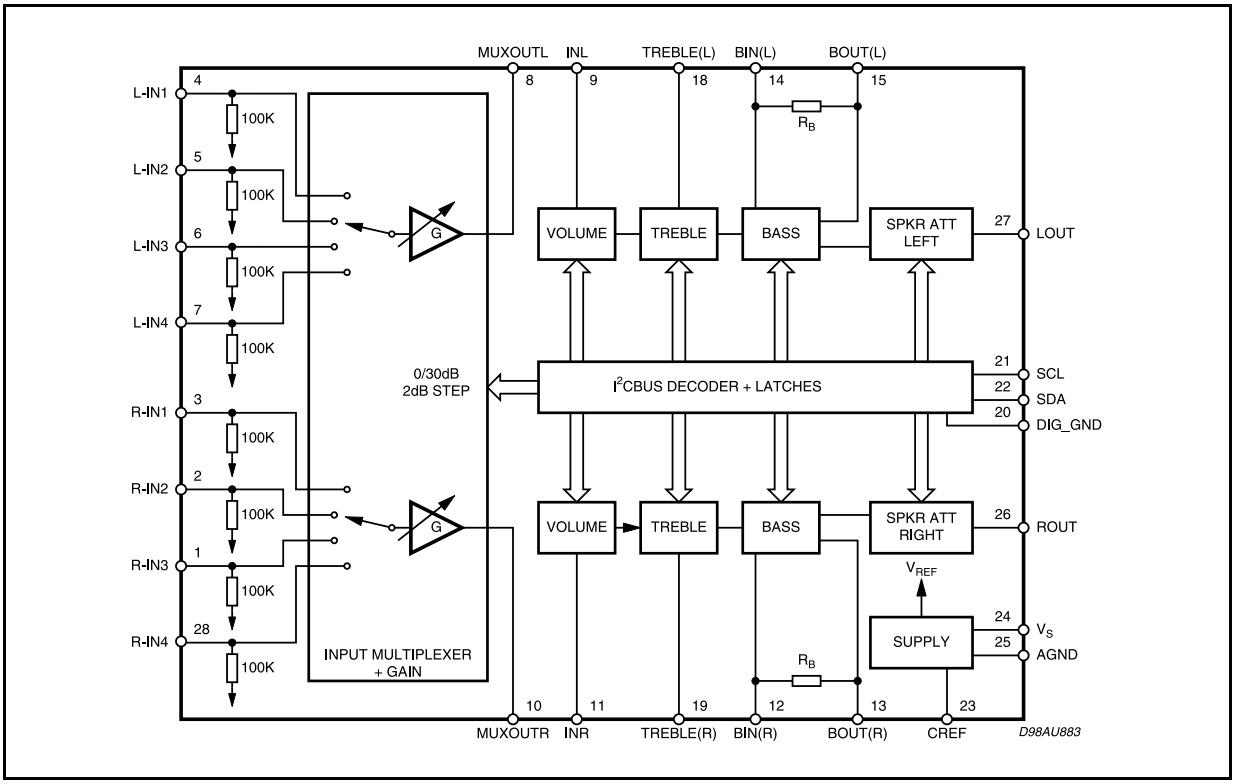


Figure 1. STAC9460 Block Diagram

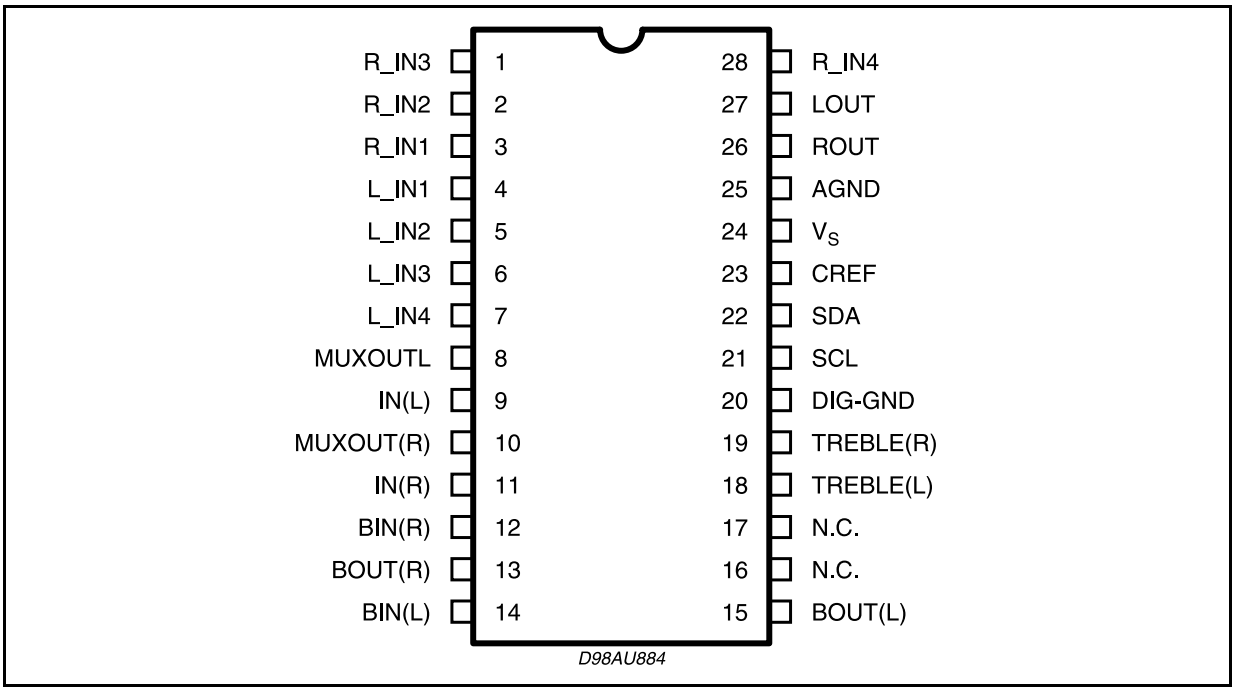


8-1-8. TDA7440D

BLOCK DIAGRAM

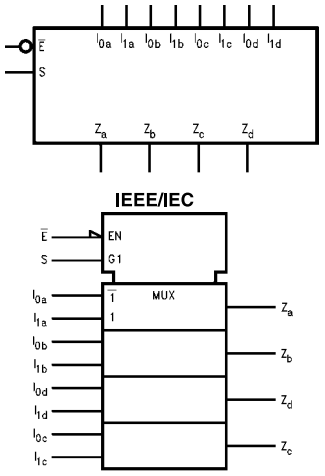


PIN CONNECTION (Top view)

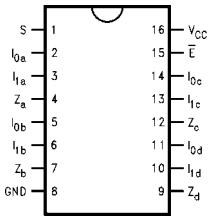


8-1-9. 74VHC157

Logic Symbols



Connection Diagram

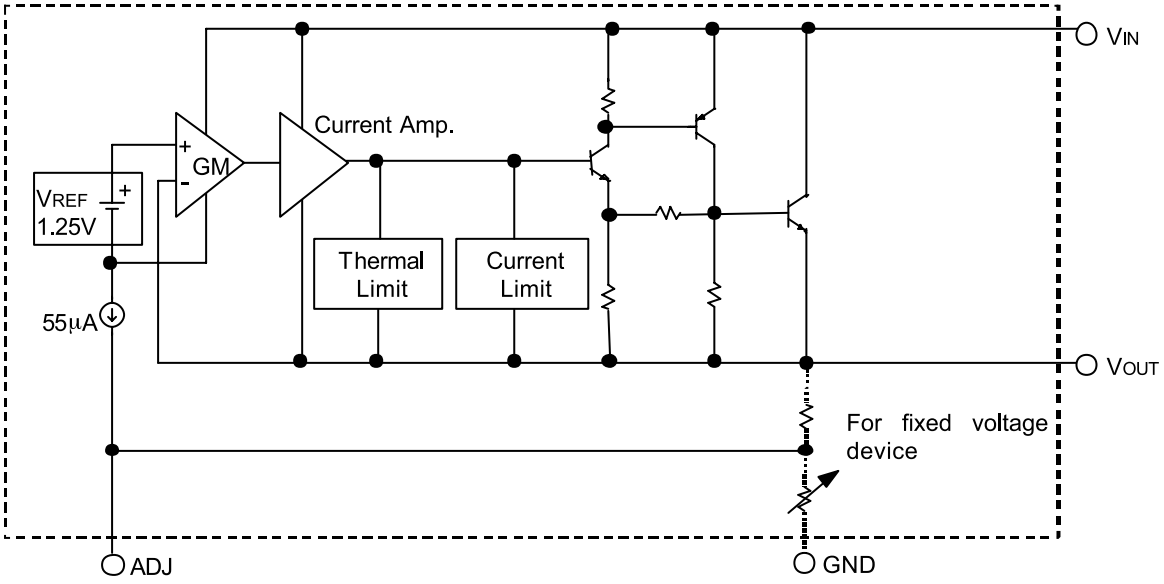


Pin Descriptions

Pin Names	Description
I_{0a}ñI_{0d}	Source 0 Data Inputs
I_{1a}ñI_{1d}	Source 1 Data Inputs
$\overline{E}$	Enable Input
S	Select Input
Z_añZ_d	Outputs

8-1-10. AIC1117A

■ BLOCK DIAGRAM



■ PIN DESCRIPTIONS

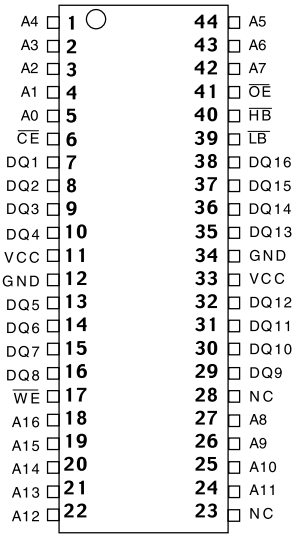
ADJ PIN - Providing V_{REF}=1.25V (typ.) for adjustable V_{OUT}. $V_{REF}=V_{OUT}-V_{ADJ}$ and I_{ADJ}=55μA (typ.)
(GND PIN - Power ground.)

VOUT PIN - Adjustable output voltage.

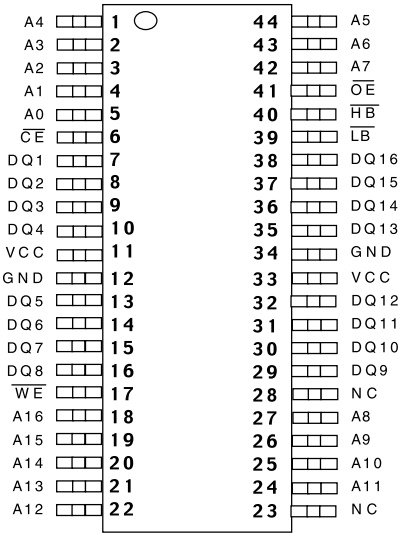
VIN PIN - Power Input.

PIN ASSIGNMENT

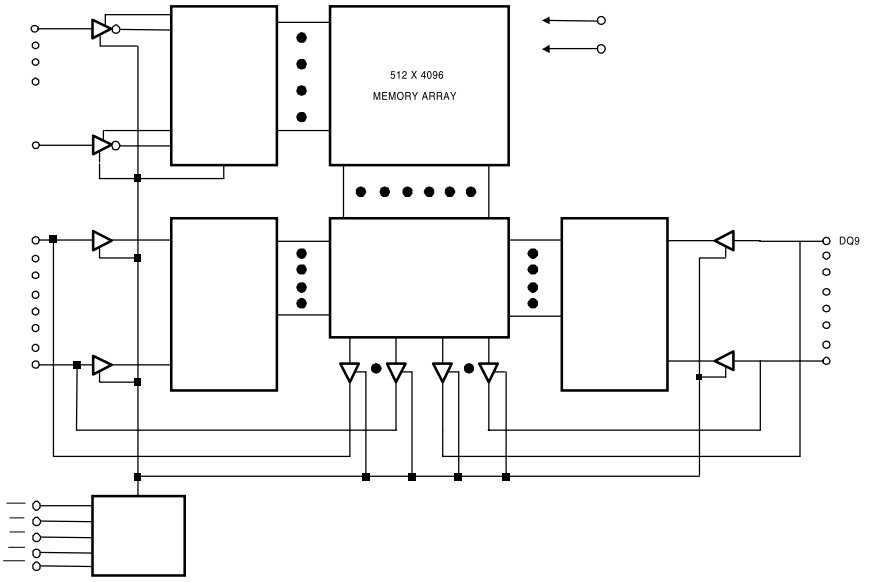
SOJ Top View



TSOP (TypeII) Top View



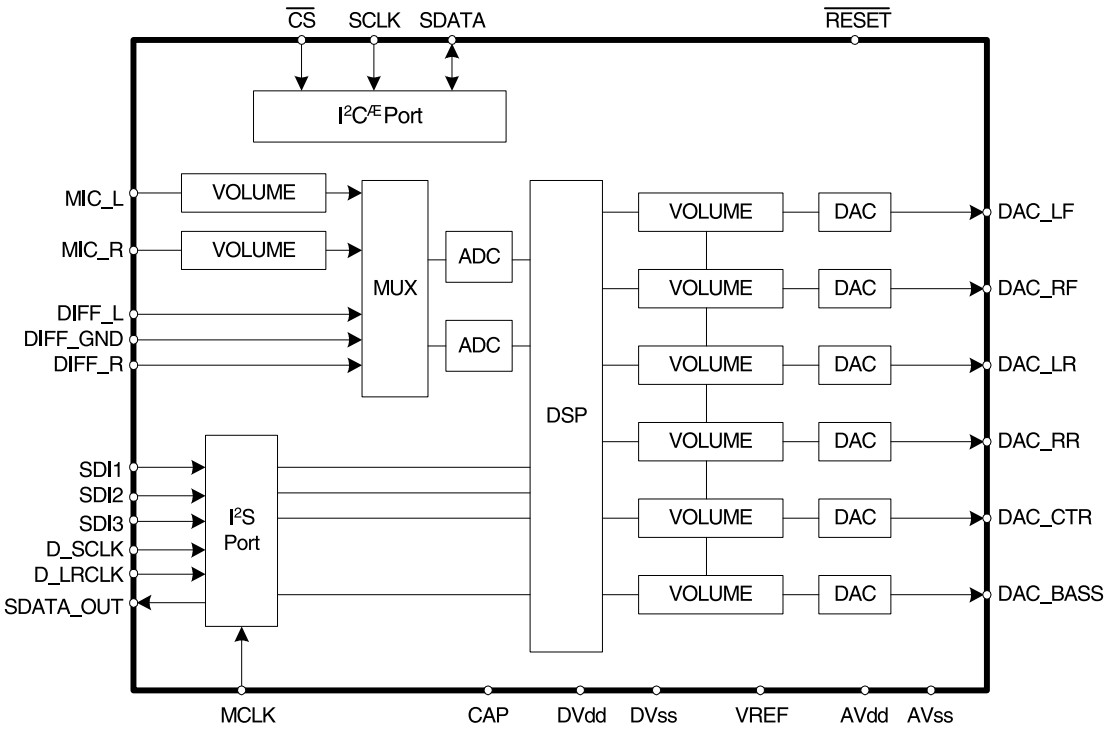
Block Diagram



Pin Descriptions

Pin No.	Symbol	Description
1 - 5, 18 - 22, 24-27, 42 - 44	A0 - A16	Address Inputs
6	$\overline{CE}$	Chip Enable Input
7 - 10, 13 - 16, 29 - 32, 35 - 38	DQ1 - DQ16	Data Inputs/Outputs
17	$\overline{WE}$	Write Enable Input
39	$\overline{LB}$	Lower Byte Enable Input (DQ1 to DQ8)
40	$\overline{HB}$	Higher Byte Enable Input (DQ9 to DQ16)
41	$\overline{OE}$	Output Enable Input
11, 33	VCC	Power
12, 34	GND	Ground
23, 28	NC	No Connection

8-1-12. STAC9460



ES60X8 PINOUT DIAGRAM

The identical device pinouts for the ES6008, ES6018, ES6028 and ES6038 are shown in Figure

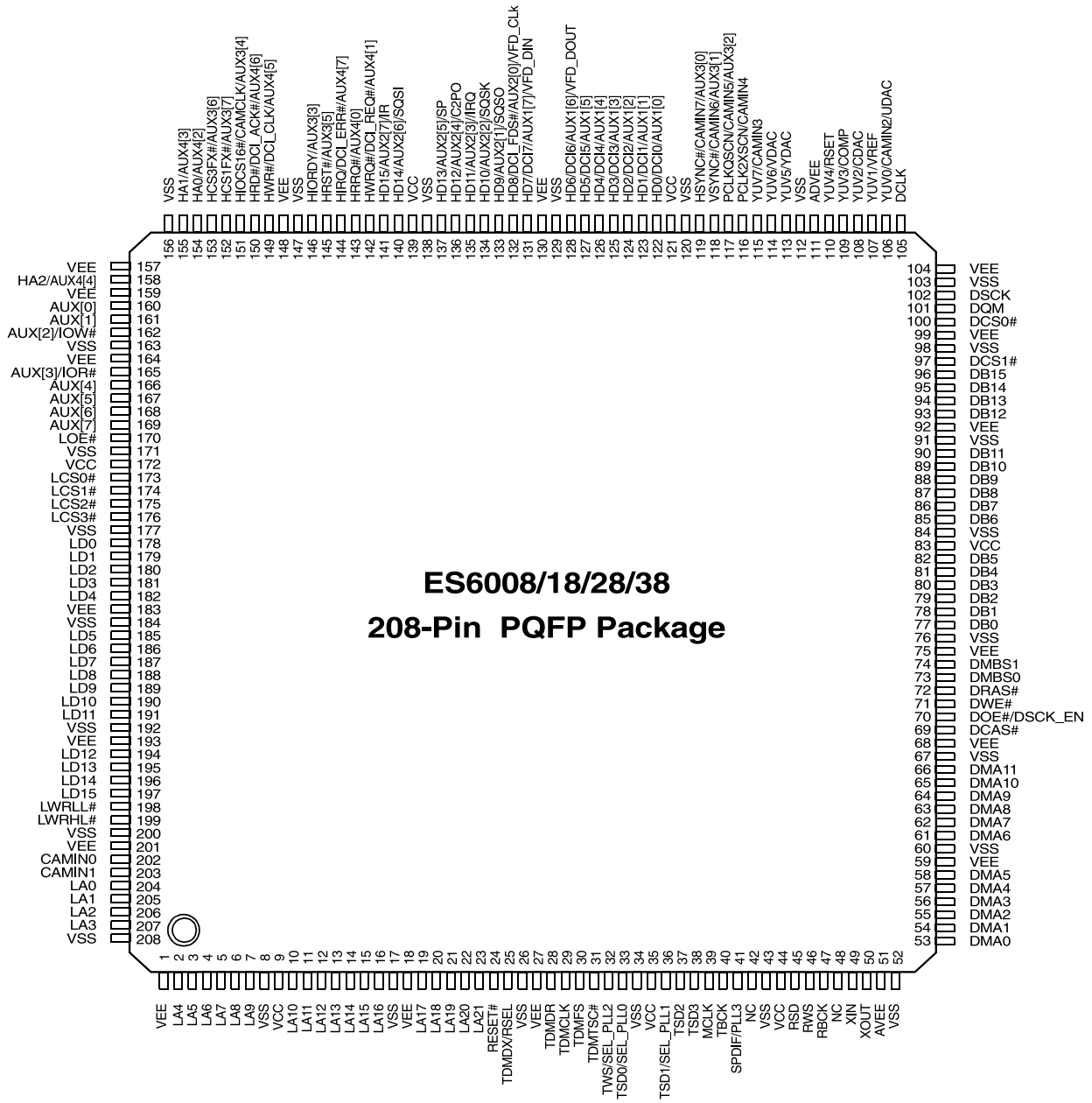


Figure ES60x8 Pinout

ES60X8 PIN DESCRIPTION

Table 1 lists the identical pin descriptions for the ES6008, ES6018, ES6028 and ES6038.

Table 1 ES60x8 Pin Description

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>VEE</td><td>1,18, 27, 59, 68, 75, 92, 99, 104, 130, 148, 157, 159, 164, 183, 193, 201</td><td>I</td><td>I/O power supply.</td></tr>
<tr><td>VSS</td><td>8, 17, 26, 34, 43, 52, 60, 67, 76, 84, 91, 98, 103, 112, 120, 129, 138, 147, 156, 163, 171, 177, 184, 192, 200, 208</td><td>I</td><td>Ground.</td></tr>
<tr><td>LA[21:0]</td><td>23:19, 16:10, 7:2, 207:204</td><td>O</td><td>Device address output.</td></tr>
<tr><td>VCC</td><td>9, 35, 44, 83, 121, 139, 172</td><td>I</td><td>Core power supply.</td></tr>
<tr><td>RESET#</td><td>24</td><td>I</td><td>Reset input, active low.</td></tr>
<tr><td>TDMDX</td><td rowspan="2">25</td><td>O</td><td>TDM transmit data.</td></tr>
<tr><td>RSEL</td><td>I</td><td>ROM Select.
<table>
<tr><th>RSEL</th><th>Selection</th></tr>
<tr><td>0</td><td>16-bit OM R</td></tr>
<tr><td>1</td><td>8-bit ROM</td></tr>
</table></td></tr>
<tr><td>TDMDR</td><td>28</td><td>I</td><td>TDM receive data.</td></tr>
<tr><td>TDMCLK</td><td>29</td><td>I</td><td>TDM clock input.</td></tr>
<tr><td>TDMFS</td><td>30</td><td>I</td><td>TDM frame sync.</td></tr>
<tr><td>TDMTSC#</td><td>31</td><td>O</td><td>TDM output enable.</td></tr>
<tr><td>TWS</td><td rowspan="2">32</td><td>O</td><td>Audio transmit frame sync.</td></tr>
<tr><td>SEL_PLL2</td><td>I</td><td>System and DSCK output clock frequency selection is made at the rising edge of RESET#. The matrix below lists the available clock frequencies and their respective PLL bit settings.
<table>
<tr><th>SEL_PLL2</th><th>SEL_PLL1</th><th>SEL_PLL0</th><th>Clock Type</th></tr>
<tr><td>0</td><td>0</td><td>0</td><td>VCO off.</td></tr>
<tr><td>0</td><td>0</td><td>1</td><td>DCLK</td></tr>
<tr><td>0</td><td>1</td><td>0</td><td>Bypass mode</td></tr>
<tr><td>0</td><td>1</td><td>1</td><td>DCLK x 2</td></tr>
<tr><td>1</td><td>0</td><td>0</td><td>DCLK x 4.5</td></tr>
<tr><td>1</td><td>0</td><td>1</td><td>DCLK x 3</td></tr>
<tr><td>1</td><td>1</td><td>0</td><td>DCLK x 3.5z</td></tr>
<tr><td>1</td><td>1</td><td>1</td><td>DCLK x 4</td></tr>
</table></td></tr>
<tr><td>TSD0</td><td rowspan="2">33</td><td>O</td><td>Audio transmit serial data port 0.</td></tr>
<tr><td>SEL_PLL0</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>TSD1</td><td rowspan="2">36</td><td>O</td><td>Audio transmit serial data port 1.</td></tr>
<tr><td>SEL_PLL1</td><td>I</td><td>Refer to the description and matrix for SEL_PLL2 pin 32.</td></tr>
<tr><td>TSD[2]</td><td>37</td><td>O</td><td>Audio transmit serial data output 2.</td></tr>
<tr><td>TSD[3]</td><td>38</td><td>O</td><td>Audio transmit serial data output 3.</td></tr>
</table>

Table 1 ES60x8 Pin Description (Continued)

<table>
<tr><th>Name</th><th>Number</th><th>I/O</th><th>Definition</th></tr>
<tr><td>MCLK</td><td>39</td><td>I/O</td><td>Audio master clock for audio DAC.</td></tr>
<tr><td>TBCK</td><td>40</td><td>O</td><td>Audio transmit bit clock.</td></tr>
<tr><td>SPDIF</td><td rowspan="2">41</td><td>O</td><td>S/PDIF output.</td></tr>
<tr><td>SEL_PLL3</td><td>I</td><td>Clock source select.
<table>
<tr><th>SEL_PLL3</th><th>Clock Source</th></tr>
<tr><td>0</td><td>Crystal oscillator</td></tr>
<tr><td>1</td><td>DCLK input</td></tr>
</table></td></tr>
<tr><td>NC</td><td>42, 48</td><td></td><td>No connect pins. Leave open.</td></tr>
<tr><td>RSD</td><td>45</td><td>I</td><td>Audio receive serial data.</td></tr>
<tr><td>RWS</td><td>46</td><td>I</td><td>Audio receive frame sync.</td></tr>
<tr><td>RBCK</td><td>47</td><td>I</td><td>Audio receive bit clock.</td></tr>
<tr><td>XIN</td><td>49</td><td>I</td><td>Crystal input.</td></tr>
<tr><td>XOUT</td><td>50</td><td>O</td><td>Crystal output.</td></tr>
<tr><td>AVEE</td><td>51</td><td>I</td><td>Analog power for PLL.</td></tr>
<tr><td>DMA[11:0]</td><td>66:61, 58:53</td><td>O</td><td>DRAM address bus [11:0].</td></tr>
<tr><td>DCAS#</td><td>69</td><td>O</td><td>DRAM column address strobe.</td></tr>
<tr><td>DOE#</td><td rowspan="2">70</td><td>O</td><td>DRAM output enable.</td></tr>
<tr><td>DSCK_EN</td><td>O</td><td>DRAM clock enable.</td></tr>
<tr><td>DWE#</td><td>71</td><td>O</td><td>DRAM write enable.</td></tr>
<tr><td>DRAS#</td><td>72</td><td>O</td><td>DRAM row address strobe.</td></tr>
<tr><td>DMBS0</td><td>73</td><td>O</td><td>SDRAM bank select 0.</td></tr>
<tr><td>DMBS1</td><td>74</td><td>O</td><td>SDRAM bank select 1.</td></tr>
<tr><td>DB[15:0]</td><td>96:93, 90:85, 82:77</td><td>I/O</td><td>DRAM data bus [15:0].</td></tr>
<tr><td>DCS[1:0]#</td><td>97,100</td><td>O</td><td>SDRAM chip select [1:0].</td></tr>
<tr><td>DQM</td><td>101</td><td>O</td><td>Data input/output mask.</td></tr>
<tr><td>DSCK</td><td>102</td><td>O</td><td>Output clock to SDRAM.</td></tr>
<tr><td>DCLK</td><td>105</td><td>I</td><td>27 MHz clock input to PLL.</td></tr>
<tr><td>YUV0</td><td rowspan="3">106</td><td>O</td><td>YUV0 pixel output data.</td></tr>
<tr><td>CAMIN2</td><td>I</td><td>Camera input 2.</td></tr>
<tr><td>UDAC</td><td>O</td><td>Video DAC output.
<table>
<tr><th>Mode</th><th>YDAC</th><th>UDAC</th><th>VDAC</th><th>CDAC</th></tr>
<tr><td>A</td><td>Y</td><td>C</td><td>Composite</td><td>C</td></tr>
<tr><td>B</td><td>Y</td><td>Composite</td><td>Composite</td><td>C</td></tr>
<tr><td>C</td><td>Y</td><td>U</td><td>Composite</td><td>V</td></tr>
<tr><td>D</td><td>Y</td><td>U</td><td>C</td><td>V</td></tr>
</table>
Y: Luma component for YUV and Y/C processing.
C: Chrominance signal for Y/C processing.
U: Chrominance component signal for YUV mode.
V: Chrominance component signal for YUV mode.</td></tr>
</table>

Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
YUV1	107	O	YUV1 pixel output data.
VREF		I	Internal voltage reference to video DAC. Bypass to ground with 0.1 F capacitor.
YUV2	108	O	YUV2 pixel output data.
CDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV3	109	O	YUV3 pixel output data.
COMP		I	Compensation input. Bypass to ADVEE with 0.1 F capacitor.
YUV4	110	O	YUV4 pixel output data.
RSET		I	DAC current adjustment resistor input.
ADVEE	111	I	Analog power for video DAC.
YUV5	113	O	YUV5 pixel output data.
YDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV6	114	O	YUV6 pixel output data.
VDAC		O	Video DAC output. Refer to description and matrix for UDAC pin 106.
YUV7	115	O	YUV7 pixel output data.
CAMIN3		I	Camera YUV 3.
PCLK2XSCN	116	I/O	27-MHz video output pixel clock.
CAMIN4		I	Camera YUV 4.
PCLKQSCN	117	O	13.5-MHz video output pixel clock.
CAMIN5		I	Camera YUV 5.
VSYNC#	118	I/O	Vertical sync, active low.
CAMIN6		I	Camera YUV 6.
HSYNC#	119	I/O	Horizontal sync, active low.
CAMIN7		I	Camera YUV 7.
HD[5:0]	127:122	I/O	Host data I/O [5:0].
DCI[5:0]		I/O	DVD channel data I/O [5:0].
AUX1[5:0]		I/O	Aux1 data I/O [5:0].
HD[6]	128	I/O	Host data I/O [6].
DCI[6]		I/O	DVD channel data I/O [6].
AUX1[6]		I/O	Aux1 data I/O [6].
VFD_DOUT		I	VFD data output.
HD[7]	131	I/O	Host data I/O [7].
DCI[7]		I/O	DVD channel data I/O [7].
AUX1[7]		I/O	Aux1 data I/O [7:0].
VFD_DIN		I	VFD data input.
HD[8]	132	I/O	Host data bus 8.
DCI_FDS#		I/O	DVD input sector start.
AUX2[0]		I/O	Aux2 data I/O 0.
VFD_CLK		I	VFD clock input.
HD[9]	133	I/O	Host data bus line 9.
AUX2[1]		I/O	Aux2 data I/O [1] when selected.
SQSQ		I	Subcode-Q data.
HD[10]	134	I/O	Host data bus line10.
AUX2[2]		I/O	Aux2 data I/O [2] when selected.
SQSK		I	Subcode-Q clock.

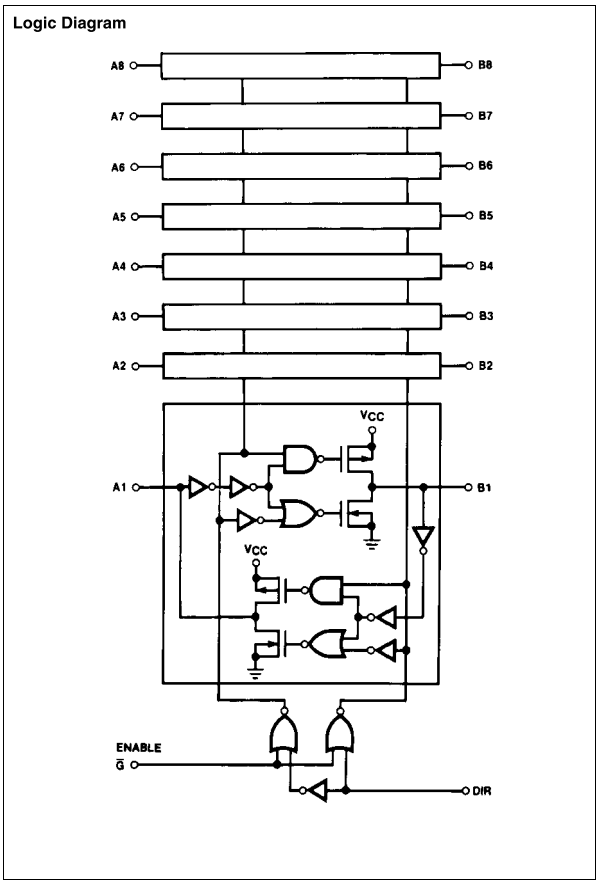
Table 1 ES60x8 Pin Description (Continued)

Name	Number	I/O	Definition
HD[11]	135	I/O	Host data bus line11.
AUX2[3]		I/O	Aux2 data I/O [3] when selected.
IRQ		O	IRQ output.
HD[12]	136	I/O	Host data bus line12.
AUX2[4]		I/O	Aux2 data I/O [4] when selected.
C2PO		I	C2PO error correction flag from CD-ROM.
HD[13]	137	I/O	Host data bus line13.
AUX2[5]		I/O	Aux2 data I/O [5] when selected.
SP		I	16550 UART serial port input.
HD[14]	140	I/O	Host data bus line14.
AUX2[6]		I/O	Aux2 data I/O [6] when selected.
SQSI		I	Subcode-Q sync.
HD[15]	141	I/O	Host data bus line15.
AUX2[7]		I/O	Aux2 data I/O [7] when selected.
IR		I	IR remote control input.
HWRQ#	142	O	Host write request.
DCI_REQ#		O	DVD control interface request.
AUX4[1]		I/O	Aux4 data I/O 1.
HRRQ#	143	O	Host read request.
AUX4[0]		I/O	Aux4 data I/O 0.
HIRQ	144	I/O	Host interrupt.
DCI_ERR#		I/O	DVD channel data error.
AUX4[7]		I/O	Aux4 data I/O 7.
HRST#	145	O	Host reset.
AUX3[5]		I/O	Aux3 data I/O 5.
HIORDY	146	I	Host I/O ready.
AUX3[3]		I/O	Aux3 data I/O 3.
HWR#	149	I/O	Host write.
DCI_CLK		I/O	DVD channel data clock.
AUX4[5]		I/O	Aux4 data I/O 5.
HRD#	150	O	Host read.
DCI_ACK#		O	DVD channel data valid.
AUX4[6]		I/O	Aux4 data I/O 6.
HIOCS16#	151	I	Device 16-bit data transfer.
CAMCLK		I	Camera port pixel clock input.
AUX3[4]		I/O	Aux3 data I/O 4.
HCS1FX#	152	O	Host select 1.
AUX3[7]		I/O	Aux3 data I/O 7.
HCS3FX#	153	O	Host select 3.
AUX3[6]		I/O	Aux3 data I/O 6.
HA[2:0]	158, 155:154	I/O	Host address bus.
AUX4[4:2]		I/O	Aux4 data I/Os [4:2].
AUX[1:0]	160	I/O	Auxiliary ports 1:0.

Table 1 ES60x8 Pin Description (Continued)

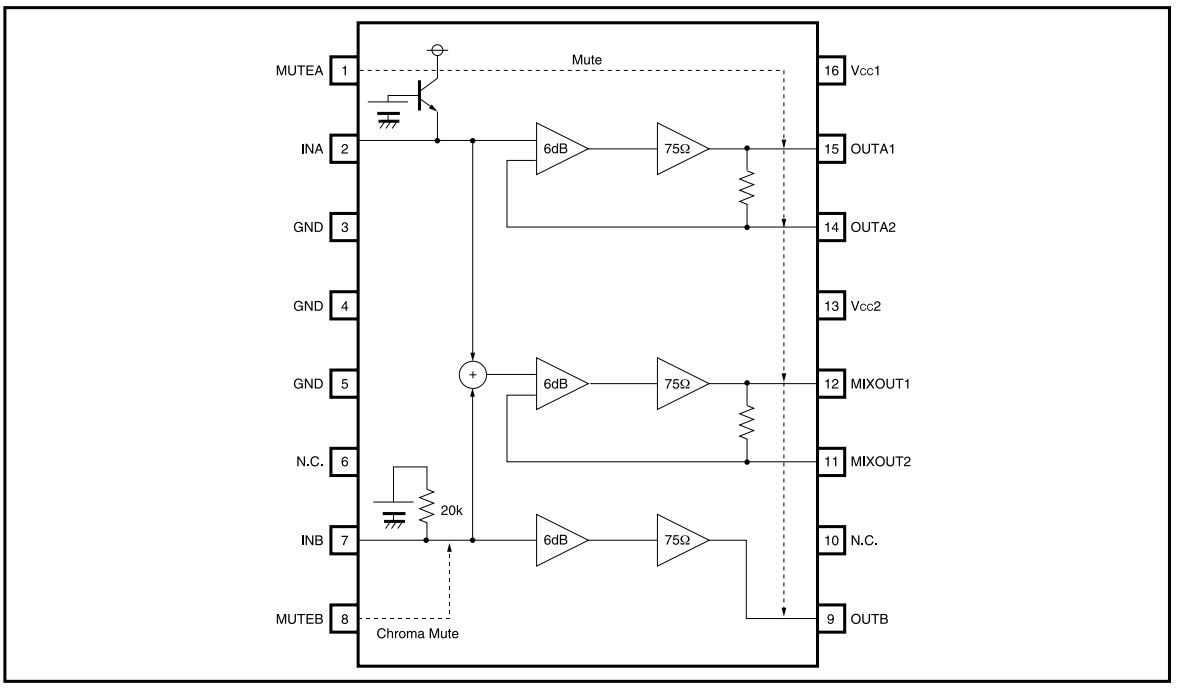
Name	Number	I/O	Definition
AUX[2]	162	I/O	Auxiliary port 2.
IOW#		O	I/O Write strobe.
AUX[3]	165	I/O	Auxiliary port 3.
IOR#		O	I/O Read strobe.
AUX[7:3]	169:166	I/O	Auxiliary ports 7:3.
LOE#	170	O	Device output enable.
LCS[3:0]#	176:173	O	Chip select [3:0].
LD[15:0]	197:194, 191:185, 182:178	I/O	EPROM device data bus.
LWRLL#	198	O	Device low-byte write enable.
LWRHL#	199	O	Device high-byte write enable.
CAMIN0	202	I	Camera YUV 0.
CAMIN1	203	I	Camera YUV 1.

8-2-2. 74HCT245

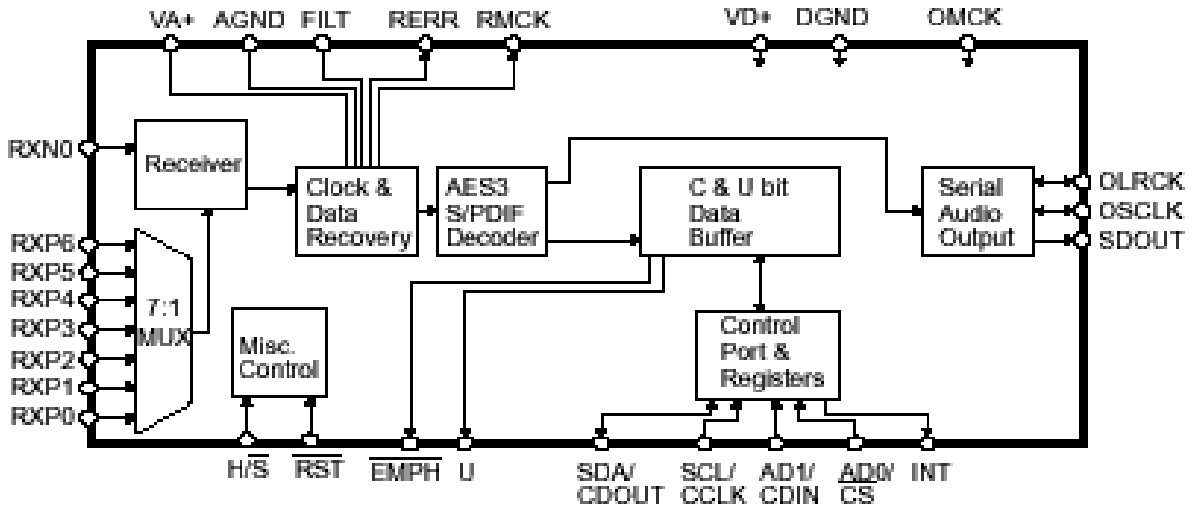


8-2-3. BA7665FS

●Block diagram

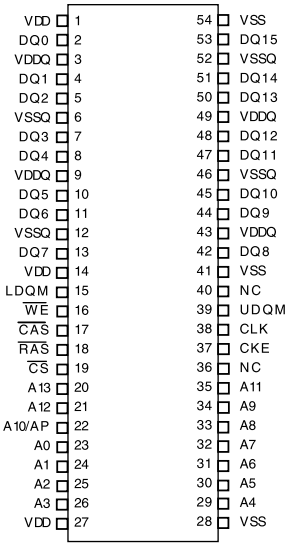


8-2-4. CS8415

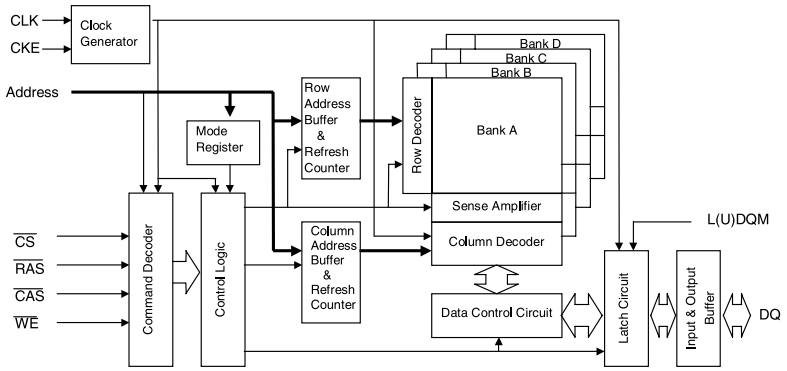


PIN ASSIGNMENT

Top View



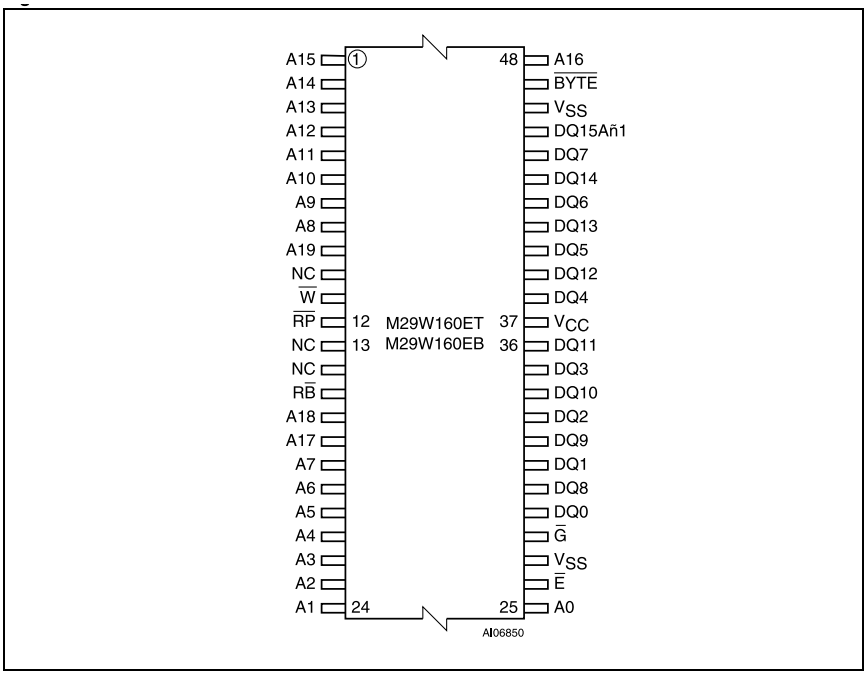
FUNCTIONAL BLOCK DIAGRAM



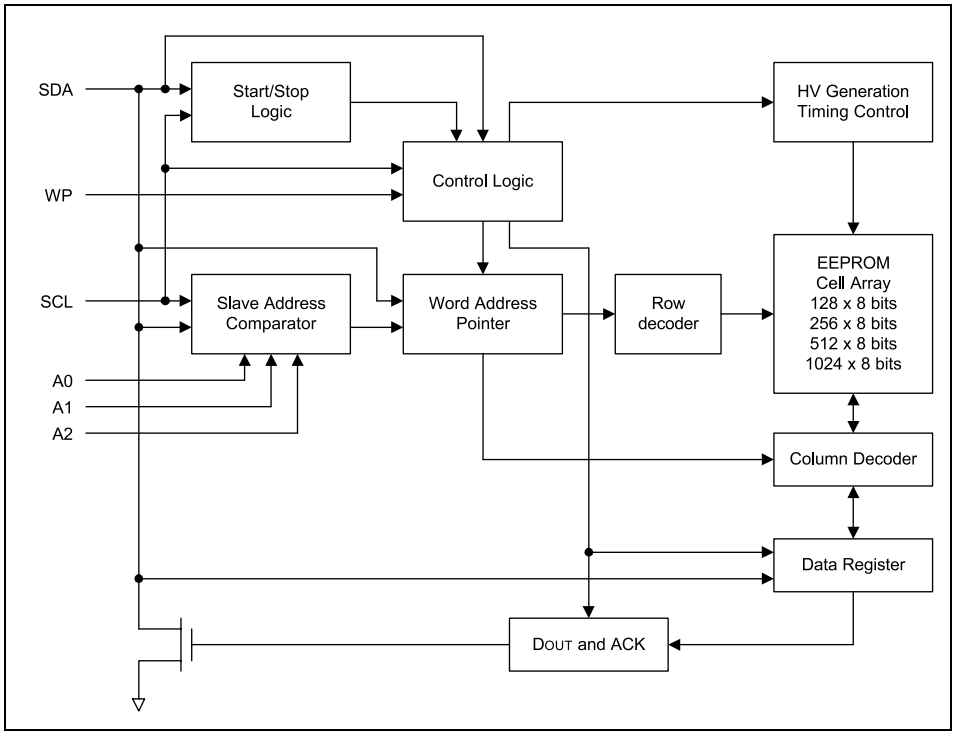
PIN FUNCTION DESCRIPTION

PIN	NAME	INPUT FUNCTION
CLK	System Clock	Active on the positive going edge to sample all inputs
$\overline{CS}$	Chip Select	Disables or enables device operation by masking or enabling all inputs except CLK , CKE and L(U)DQM
CKE	Clock Enable	Masks system clock to freeze operation from the next clock cycle. CKE should be enabled at least one cycle prior new command. Disable input buffers for power down in standby.
A0 ~ A11	Address	Row / column address are multiplexed on the same pins. Row address : RA0~RA11, column address : CA0~CA7
A12 , A13	Bank Select Address	Selects bank to be activated during row address latch time. Selects bank for read / write during column address latch time.
$\overline{RAS}$	Row Address Strobe	Latches row addresses on the positive going edge of the CLK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Column Address Strobe	Latches column address on the positive going edge of the CLK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Write Enable	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
L(U)DQM	Data Input / Output Mask	Makes data output Hi-Z, t_{SHZ} after the clock and masks the output. Blocks data input when L(U)DQM active.
DQ0 ~ DQ15	Data Input / Output	Data inputs / outputs are multiplexed on the same pins.
VDD / VSS	Power Supply / Ground	Power and ground for the input buffers and the core logic.
VDDQ / VSSQ	Data Output Power / Ground	Isolated power supply and ground for the output buffers to provide improved noise immunity.
NC	No Connection	This pin is recommended to be left No Connection on the device.

8-2-6. M29W160E



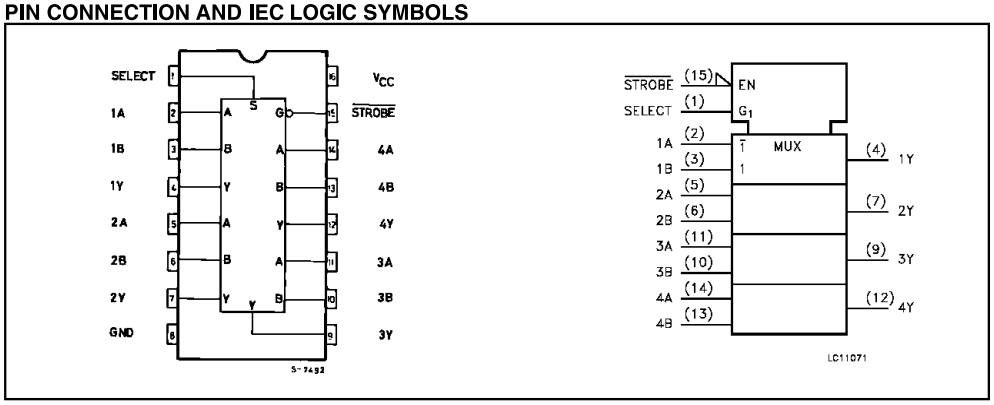
8-2-7. S524C20D21_20D41



S524C20D11/20D21/80D41/80D81 Block Diagram

8-2-8. STM_74LCX157

PIN CONNECTION AND IEC LOGIC SYMBOLS

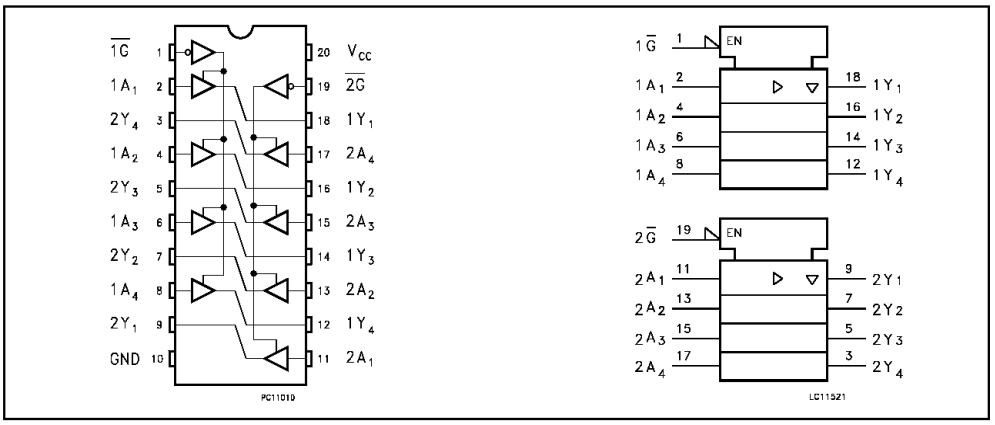


PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	SELECT	Common Data Select Inputs
2, 5, 11, 14	1A to 4A	Data Inputs From Source A
3, 6, 10, 13	1B to 4B	Data Inputs From Source B
4, 7, 9, 12	1Y to 4Y	Multiplexer Outputs
15	STROBE	Strobe Input
8	GND	Ground (0V)
16	V_{CC}	Positive Supply Voltage

8-2-9. STM_74LCX244

PIN CONNECTION AND IEC LOGIC SYMBOLS



PIN DESCRIPTION

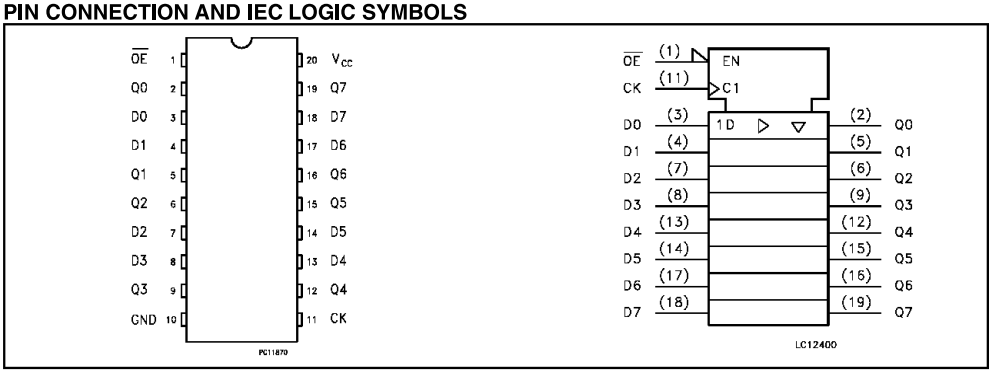
PIN No	SYMBOL	NAME AND FUNCTION
1	$\overline{1G}$	Output Enable Input
2, 4, 6, 8	1A1 to 1A4	Data Inputs
9, 7, 5, 3	2Y1 to 2Y4	Data Outputs
11, 13, 15, 17	2A1 to 2A4	Data Inputs
18, 16, 14, 12	1Y1 to 1Y4	Data Outputs
19	$\overline{2G}$	Output Enable Input
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT		OUTPUT
$\overline{G}$	An	Yn
L	L	L
L	H	H
H	X	Z

X : Don't Care
Z : High Impedance

PIN CONNECTION AND IEC LOGIC SYMBOLS



PIN DESCRIPTION

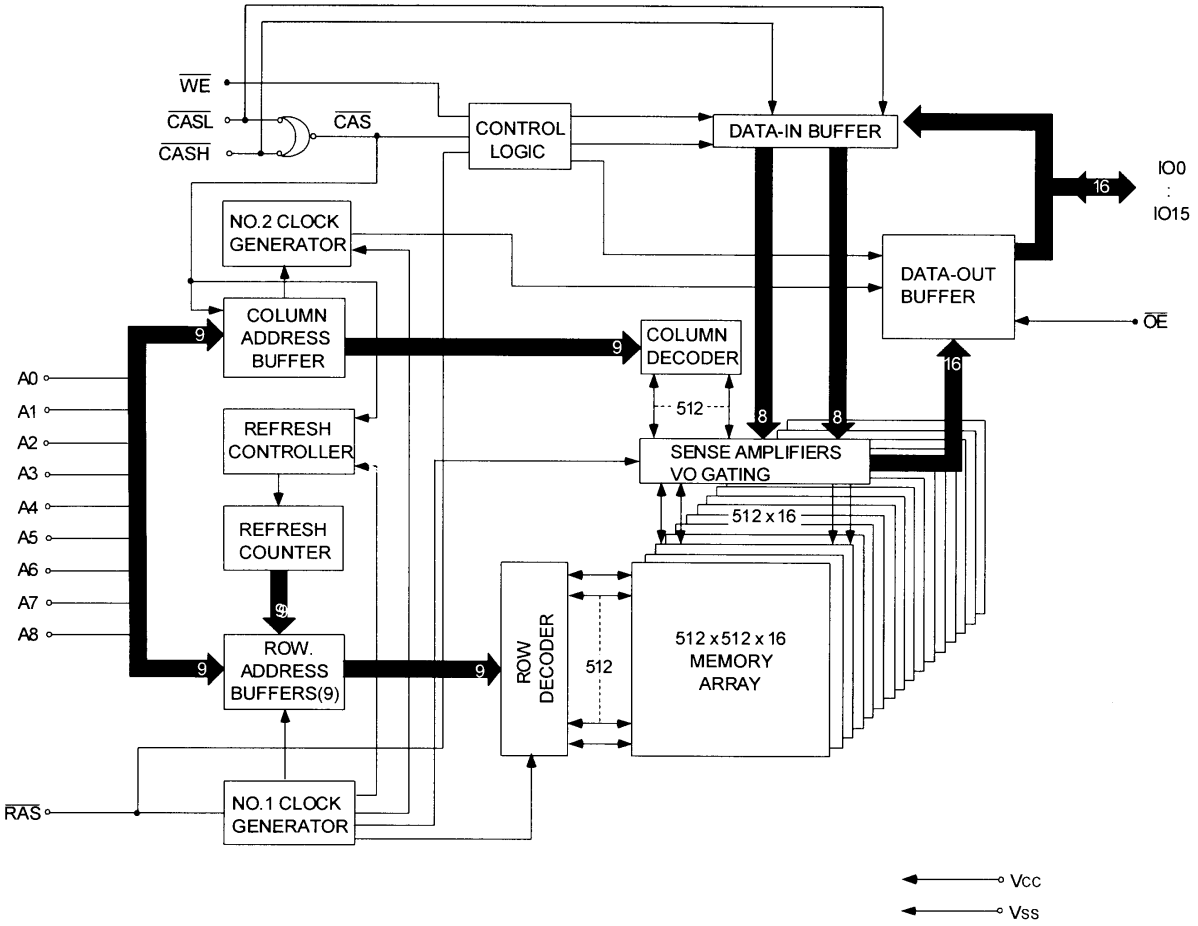
PIN No	SYMBOL	NAME AND FUNCTION
1	OE	3 State Output Enable Input (Active LOW)
2, 5, 6, 9, 12, 15, 16, 19	Q0 to Q7	3-State Outputs
3, 4, 7, 8, 13, 14, 17, 18	D0 to D7	Data Inputs
11	CK	Clock Input (LOW to HIGH, edge triggered)
10	GND	Ground (0V)
20	V_{CC}	Positive Supply Voltage

TRUTH TABLE

INPUT			OUTPUT
$\overline{OE}$	CK	D	Q
H	X	X	Z
L	↓	X	NO CHANGE
L	↑	L	L
L	↑	H	H

X : Don't Care
Z : High Impedance

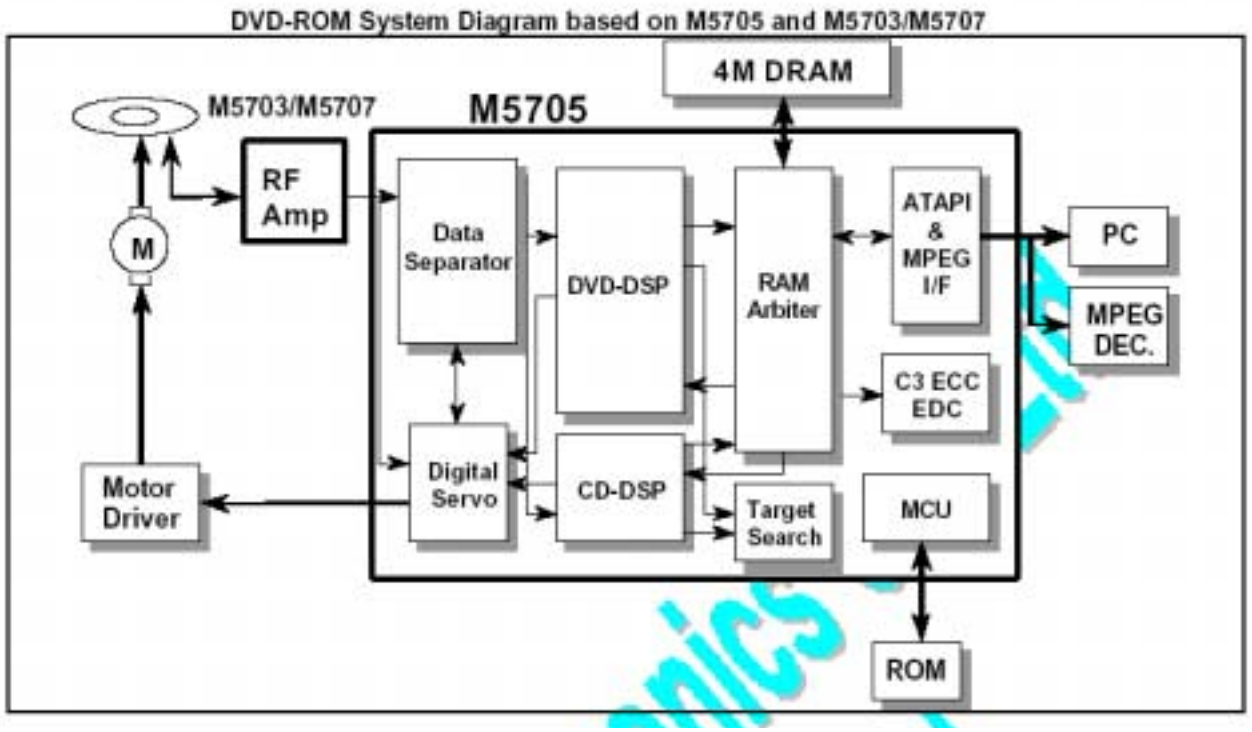
FUNCTIONAL BLOCK DIAGRAM



PIN DESCRIPTIONS

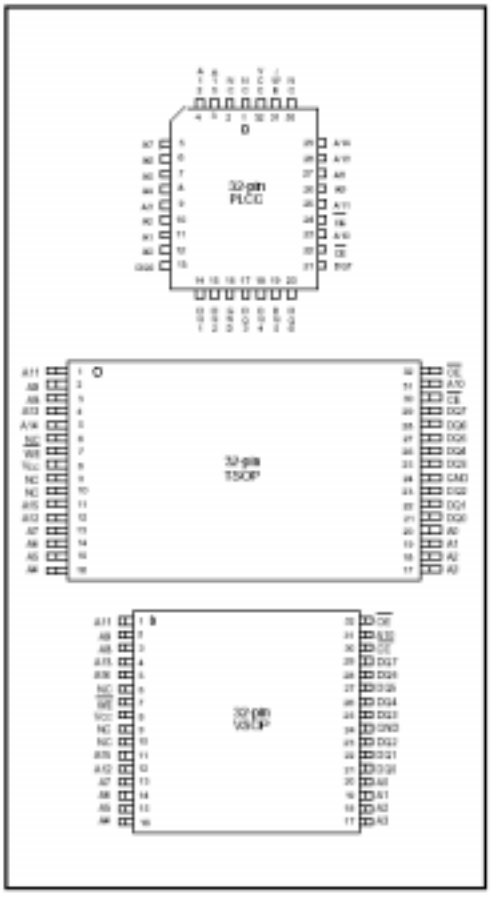
PIN NO.	SYM.	TYPE	DESCRIPTION
16~19,22~26	A0~A8	Input	Address Input
14	$\overline{RAS}$	Input	Row Address Strobe
28	$\overline{CASH}$	Input	Column Address Strobe/Upper Byte Control
29	$\overline{CASL}$	Input	Column Address Strobe/Lower Byte Control
13	$\overline{WE}$	Input	Write Enable
27	$\overline{OE}$	Input	Output Enable
2~5,7~10,31~34,36~39	I/O0 ~ I/O15	Input/Output	Data Input/Output
1,6,20	Vcc	Supply	Power, 5V
21,35,40	Vss	Ground	Ground
11,12,15,30	NC	-	No Connect

8-3-2. M5705

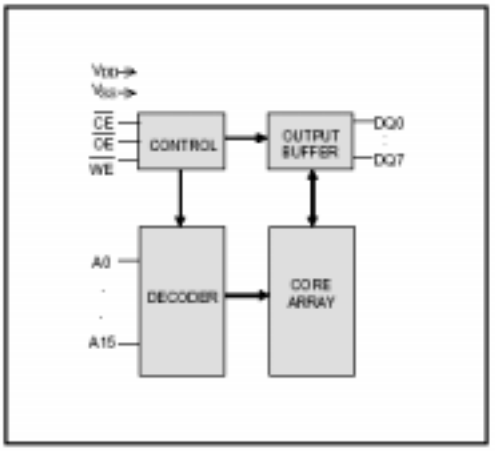


8-3-3. W29EE512F1

PIN CONFIGURATIONS



BLOCK DIAGRAM



PIN DESCRIPTION

SYMBOL	PIN NAME
A0–A15	Address Inputs
DQ0–DQ7	Data Inputs/Outputs
$\overline{CE}$	Chip Enable
$\overline{OE}$	Output Enable
$\overline{WE}$	Write Enable
VCC	Power Supply
GND	Ground
NC	No Connection

8-4 MICOM PORT ASSIGNMENT

HT-DB300/350/750 PORT ASSIGNMENT REV3

NO	PORT	NAME	I/O	TYPE	FUNCTION	NO	PORT	NAME	I/O	TYPE	FUNCTION
1	P16	CK1	O		F1,F2/TU/EXP/CODEC/DAB	51	PIX0	VPP			-36V
2	P17	DO1	O		F1,F2/TU/EXP/CODEC/DAB	52	PC4	S9	O		VFD SEG9(DVD1)
3	P30	FULT	O	INT	M62446(SM7347) LATCH	53	PC5	S10	O		VFD SEG10(DVD2)
4	P31	DI1	I	INT	M66010 DATA IN	54	PC6	S11	O		VFD SEG11(DVD3)
5	P32	CE1	O	INT	M66010 LATCH	55	PC7	S12	O		VFD SEG12(DVD4)
6	P33	CE2	O	INT	LC72131 LATCH	56	PD0	S13	O		VFD SEG13(DVD5)
7	P34	DI2	I	INT	LC72131 DATA IN	57	PD1	S14	O		VFD SEG14(NEW DSP)
8	P35	SS	O	INT	DSP CHIP SELECT	58	PD2	S15	O		VFD SEG15(DAB)
9	P36	SCK	O	INT	DSP CLOCK	59	PD3	S16	O		VFD SEG16(Full Range)
10	P37	D.RESET	O	INT	DVD RESET	60	PD4	S17	O		VFD SEG17(RGB/YCbCr)
11	RES	RESET	I		MICOM RESET	61	PD5	S18	O		VFD SEG18(Opt.Output)
12	XT1	XT1	I		NC(PULL UP)	62	PD6	S19	O		VFD SEG19(300/750)
13	XT2	XT2	O		NC(OPEN)	63	PD7	S20	O		VFD SEG20(WIDE)
14	VSS1	GND			GND	64	PE0	S21	O		VFD SEG21
15	CF1	CF1	I		10MHZ OSC IN	65	PE1	S22	O		VFD SEG22
16	CF2	CF2	O		10MHZ OSC OUT	66	PE2	S1	O		VFD SEG1
17	VDD1	VDD1			VDD 5V	67	PE3	S2	O		VFD SEG2
18	P80	AD1	I	AD	KEY A/D 1	68	PE4	S3	O		VFD SEG3
19	P81	RDS-DI	I	AD	RDS DATA IN	69	PE5	S4	O		VFD SEG4
20	P82	NC	I	AD	NC(PULL DOWN)	70	PE6	OPT IN	I		OPTION IN(PULL DOWN)
21	P83	NC	I	AD	NC(PULL DOWN)	71	PE7	NC			NC(PULL DOWN)
22	P84	NC	O	AD	NC(PULL DOWN)	72	VDD4	VDD4			VFD 5V
23	P85	NC	O	AD	NC(PULL DOWN)	73	PF0	HP SENS	I		HEADPHONE SENS
24	P86	NC	O	AD	NC(PULL DOWN)	74	PF1	P ON	O		POWER ON
25	P87	NC	O	AD	NC(PULL DOWN)	75	PF2	EVR.IN	I		VOLUME UP
26	P70	RDS-CK	I	INT	RDS CLK IN/DAB REQUEST	76	PF3	EVR.IN	I		VOLUME DOWN
27	P71	RXD	I	INT	RXD	77	PF4	P SENS	I		POWER SENS
28	P72	PREQ	I	INT	DSP REQUEST	78	PF5	NC	O		NC(PULL DOWN)
29	P73	REMO	I	INT	REMOCON IN	79	PF6	NC	O		NC(PULL DOWN)
30	T0	G1	O		VFD GRID 1	80	PF7	NC	O		NC(PULL DOWN)
31	T1	G2	O		VFD GRID 2	81	PG0	NC	O		NC(PULL DOWN)
32	T2	G3	O		VFD GRID 3	82	PG1	NC	O		NC(PULL DOWN)
33	T3	G4	O		VFD GRID 4	83	PG2	NC	O		NC(PULL DOWN)
34	T4	G5	O		VFD GRID 5	84	PG3	NC	O		NC(PULL DOWN)
35	T5	G6	O		VFD GRID 6	85	PO0	NC	O		NC(OPEN)
36	T6	G7	O		VFD GRID 7	86	PO1	LED1	O		Volume LED ON/OFF
37	T7	G8	O		VFD GRID 8	87	PO2	LED2	O		Volume DIMMER
38	T8	G9	O		VFD GRID 9	88	PO3	LED3	O		P/ON LED(Active"L")
39	T9	G10	O		VFD GRID 10	89	VSS2	GND			GND
40	T10	G11	O		VFD GRID 11	90	VDD2	VDD2			VDD 5V
41	T11	NC	O		NC(PULL DOWN)	91	P04	NC	O		NC(OPEN)
42	T12	NC	O		NC(PULL DOWN)	92	P05	LED4	O		H/P Surr LED
43	T13	NC	O		NC(PULL DOWN)	93	P06	LED5	O		Hall Surr LED
44	T14	NC	O		NC(PULL DOWN)	94	P07	LED6	O		Auto SETUP LED
45	T15	NC	O		NC(PULL DOWN)	95	P10	DAB CS	O		DAB Chip Selector
46	VDD3	VDD3			VFD 5V	96	P11	SI	I		DSP DATA IN (DSP:SO)
47	PC0	S5	O		VFD SEG5(TUNER1)	97	P12	SO	O		DSP DATA OUT(DSP:SI)
48	PC1	S6	O		VFD SEG6(TUNER2)	98	P13	TXD	O		TXD
49	PC2	S7	O		VFD SEG7(TUNER3)	99	P14	STB	O		STB
50	PC3	S8	O		VFD SEG8(RDS)	100	P15	ACK	I		ACK

<UPDATE CONNECTION>

1	97	CLK
2	96	DO
3	95	DI
4	90	VDD
5	89	GND
6	11	RESET

<PACK CONNECTION>

DVD-PACK		MICOM
P-RXD	<--	P-TXD
P-TXD	-->	P-RXD
P-ACK	<--	P-STB
P-STB	-->	P-ACK

* PORT EXPANDER

HT-DB300/350/750 EXPANDER REV3

M66010 (EXPANDER)

NO	PORT	NAME	I/O	TYPE
1	DO	DO1	O	E-DATA (MICOM : DI1)
2	DI	DI1	I	M-DATA (MICOM : D01)
3	CLK	CK1	I	M-CLK
4	CE	CE1	I	LATCH
5	VCC	VCC		MICOM 5V
6	CLS	CLS	I	MICOM 5V
7	GND	GND		GND
8	D24	SEL_1	O	PASS-THROUGH(=H)
9	D23	MIC-S	I	MIC-SENCE (Active H)
10	D22	NC	O	NC
11	D21	V-SW1	O	A/V SW1
12	D20	V-SW2	O	A/V SW2
13	D19	RGB	O	V-AV SEL
14	D18	AV1	O	V-CTRL1(VIDEO INPUT SELECTION)
15	D17	AV2	O	V-CTRL2(VIDEO INPUT SELECTION)
16	GND	GND		GND
17	D16	F-L	0	FRONT L-CH GAIN ADJ.
18	D15	F-R	0	FRONT R-CH GAIN ADJ.
19	D14	C	0	CENTER-CH GAIN ADJ.
20	D13	R-L	0	REAR L-CH GAIN ADJ.
21	D12	R-R	0	REAR R-CH GAIN ADJ.
22	D11	DAB-CON	O	DAB SPDIF SELECTOR
23	D10	F.B SNS	I	FAN MALFUNCTION SENSE (NC)
24	D9	TUNED	I	TUNED (Active L)
25	D8	ST	I	STEREO (Active L)
26	D7	H-M	O	H/P MUTE
27	D6	COD RESET	O	CODEC RESET (=L)
28	D5	SETUP MIC	O	SETUP MIC INSERT (=H)
29	D4	SCART_M	O	Scart Mute
30	D3	DAB RESET	O	DAB RESET (=L)
31	D2	PLD-RES	O	PLD RESET (=L)
32	D1	PRO	I	PROTECTION (Active H)

M62446 (FUNCTION IC)

NO	PORT	NAME
1	OUT4	C/MUTE
2	OUT3	R/MUTE
3	OUT2	F/MUTE
4	OUT1	AMP-ON